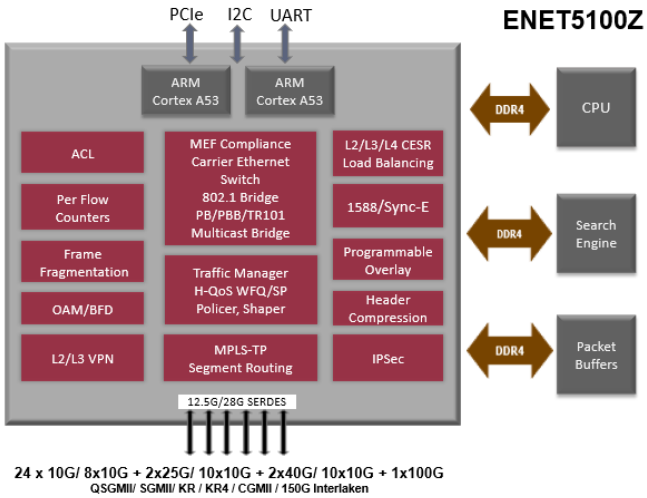
ENET Switch Router Flow Processor Family

Ethernity's ENET switch-router flow processors are integrated into Xilinx FPGAs to provide packet processing of Layer 2/3/4 traffic with complex traffic management. The family is uniquely positioned to deliver an optimal solution for the Carrier Ethernet Switch, MSAN (Multi Service Access Node), LTE base station, mobile backhaul, and Ethernet switch and router markets. It is ideal for aggregation platforms and demarcation device applications, such as SD-WAN, uCPE, and Multiaccess Edge Computing.

ENET switch controllers are compliant with OpenFlow and Metro Ethernet Forum specifications. They are SDN/NFV-ready and support new frame manipulation on-the-fly in the programmability abstraction layer.



Customizable Network Interfaces

Product Highlights

- Flexible interface support that can be customized to any port or interface configuration
- Enhanced flexibility, configurability, and programmability including field upgradeability
- Deterministic performance – 20/40Gbps
- Up to 1M flows
- Integrated dual-core ARM Cortex-9 CPU
- Integrated OF 1.4 agent for support on HW and driver level
- Carrier Ethernet switching
- MEF-compliant advanced hierarchical Traffic Manager per virtual port
- GRE, GTP, IPinIP, VxLAN tunneling protocols
- Extended buffer space through DDR3
- OAM/CFM – 802.1ag/Y.17131
- IPSec integration-ready

Ethernity Networks • www.ethernitynet.com • email: info@ethernitynet.com
13A HaMelacha Street, Lod Industrial Park, Israel 7152025 • Tel: +972-8-9150392 Fax: +972-8-9150376

Specifications

General

- FPGA Flow Based processor
- L2/3/4 flow classification, hierarchical ACL
- Search engine with up to 1M entries
- Carrier Ethernet Switch:
  - L2 multicast up to 8K active bridge multicast groups
  - L2 unicast up to 256K MAC table
  - Hardware MAC Learning
  - 802.3 Bridging
  - 802.1Q VLANs
  - 802.3ad LAG
  - 802.1ad QinQ
- IP Routing/Gateway
  - IPv4 / IPv6 Routing
  - CGNAT/NAPT
  - Virtual Routers
  - Policy-Based Forwarding
- MPLS
  - MPLS LER/LSR
  - Segment Routing
- L2/L3 VPN & Tunneling:
  - GRE/ NVGRE/ VxLAN
  - PPPoE/L2TP/L2TPv3
  - 6VPE
  - VPLS/H-VPLS (E-LAN)
  - VPWS (E-Line)
- Five-level packet header & payload manipulation and marking: MPLS/PBB/QinQ (PB)
- LAG (L2, L3, L4 distribution)
- ERPS, ELPS
- Y.1731, RFC2544, 802.1ag, OAM
- Jitter buffer/reordering engine/EFM bonding
- IEEE 1588v2, Sync E
- Wire speed NAT/NATPT
- TR101-TR-156
- Header compression and fragmentation
- Zero-time port switchover
- Hierarchical traffic management

Classification and Filtering

- Packet classification based on first 196 bytes in packet (can be extended)
- Configurable per flow functions: filtering, trapping, mirroring, packet editing, QoS remarking
- Control filtering and forwarding
- Hierarchical ACL and mask configuration per field
- Rate dependent filters (e.g., limit rate of ingress IGMPv3 packets)
- Configurable control of MAC address learning per port/VLAN
- Configurable packet type rate limitation (e.g., rate of IGMPv3 and OAM packets)

Switching

- L2 PBE switching compliant with IEEE 802.1ad
- Configurable per flow learning and forwarding profile
- Switching based on inner MAC and combination of network tags and/or outer MAC and combination of network tags
- TR-101

OAM

- Hardware support for CFM compliant with 802.1ag
- Support for four ME levels in compliance with TR-101 and TR-156
- Rate limitation and filtering of OAM messages to prevent network attacks
- L2/L3/L4 control packets classifier for both user and network L2 control protocol
- Integrated packet generator and analyzer to support OAM packet generation and analysis per Y.1731**,** including per-flow BERT
- Hardware processing for L2, L3 loop backs (swap L2 SA/DA, swap L3 SA/DA)
- Hardware fast-protecting switching within microseconds

Interfaces

- 8 x 10G SERDES supporting 4/8 x KR/QSGMII/SGMII (1/2.5/10GbE)
- Up to 32 x 1G through 8 x QSGMII
- Up to 8 x DDR3
- Additional options available for programming

Packet Editing

- Bit- and byte-level editing of first 128 bytes, including QoS remarking, byte counts, sequence ID and DSCP, and FCS calculation
- Header modification up to 48 bytes (push/pop/modify) for VLAN
- L2 and L3 loop backs, including swap of MAC SA and DA, swap of IP

CPU

- Embedded dual core ARM A9

Software

- OF 1.3 agent integrated on driver level
- OpenWrt Chaos Calmer
- 3d Party SW HAL implementation

Ordering Options

Part number	Description
ENET3850Z	6G switch router flow processor with 4 x 1/2.5G interfaces
ENET4200Z	12G switch router flow processor with 4 x 1/2.5/10G interfaces
ENET4840Z	40G switch router flow processor with 8 x 1/2.5/10G interfaces
ENET5100Z	100G switch router flow processor with 24 x 10G interfaces