# PON OLT MAC SoC

## With Support for XGS-PON and GPON

Ethernity's PON OLT MAC SoC is an efficient, compact Optical Line Terminal (OLT) design integrated on an FPGA SoC that is fully compliant with the ITU standard specification, and which exploits the benefits of XGS-PON and/or GPON to the maximum.

The SoC can support 4 x XGS-PON or 8 x GPON. Ethernity's implementation of an XGS-PON OLT MAC enables a shared optical communication link between up to 128 endpoint ONUs via Passive Optical Network (PON) and supports a symmetric 9.9Gbps rate in both upstream and downstream directions. When integrated with a simple switch and CPU, a variety of FTTx solutions are easily achieved: FTTH, FTTb, FTTc, and others.

### Product Highlights

- 4 x XGS-PON or 8 x GPON
- Integrated Burst-Mode Clock Data Recovery (BM-CDR)
- Integrated HW DBA engine with very low latency and fast response time
- AES encryption engine
- 18K virtual ports (XGEM-PortIDs) per PON Channel
- 1,152 AllocIDs (9 per ONU)
- Segmentation And Reassembly (SAR) at line rate
- Jumbo packet Support

This OLT MAC supports thousands of ALLOC-IDs and XGEM-PORTs (see table below) along with FEC error correction, AES encryption, and time-of-day synchronization. Dynamic Bandwidth Allocation (DBA) allows control of upstream traffic from ONUs, while Burst-mode Clock Data Recovery (BCDR) is implemented on the FPGA to compensate for phase variation between different ONUs.

| | XGS-PON | GPON |
|---|---|---|
| Number of ONUs | 128 | 64 |
| Number of ALLOC-IDs | 1152 | 1152 |
| Number of XGEM-PORTs | 18K | 4K |
| FEC | RS(248,216) | RS(255,239) |

# *Specifications*

**DBA**

- Persistent DBA utilization of > 99%
- Convergence time: a single DBA Cycle, no dependency between DBA cycles
- Fully Status Reporting: all Alloc-IDs are probed for DBRu every DBA cycle
- Minimal DBA-Cycle: 250µs (2 x 125µs) with 1152 Alloc-IDs, 128 ONUs
- Fully HW-Based DBA engine
- Up to 1152 Alloc-IDs
- Minimum-Guaranteed per AllocID + a configurable share in Best-Effort, including setting a maximum limit on Best-Effort share
- Supports 5 T-CONT types (Type-1, … Type-5)

**Interfaces**

- 8 x 10G SERDESs circuitry supporting up to 8 GPON i/f or 4 x XGS-PON
- 4x10GE SFP+ transceiver
- 1xSGMII control I/F
- 1x UART for debug + R&D
- 1 PPS for precision time stamping

**Ethernet**

- Jumbo frame support
- IP packet fragmentation (DS) and reassembly (US) through external 4 x 16-bit DDR4.
- RMON
- VID to X/GEM Port ID/LLID mapping function
- MAC+VID to X/GEM Port ID/LLID mapping function

**SW KIT**

- PON API software is available with the SoC for integration with a higher level software stack

**Customization**

- OLT XGS-PON/GPON MAC design can be ported to any FPGA to support SFP pluggable or higher end port capacity on a larger FPGA device

**XGS-PON OLT MAC SoC Ordering Options**

| Product Name | Product Description* |
|---|---|
| ENET-P104X | 4 x XGS-PON with 4 x 10GE interfaces |
| ENET-P008G | 8 x GPON with 8 x 2.5GE interfaces |

*Additional options with different port densities are available upon request.